Atty. Docket No. PIA31223/DBE/US
Serial No: 10/751,212

Amendments to the Figures

FIG. 1 has been amended by adding the label "(RELATED ART)" below the Figure, as required by the Examiner. In addition, FIG. 3A (which is an enlarged sectional view of an Au bump formed on a bond pad of the chip shown in FIG. 2) has been amended by adding bond pad 208, and Cu pattern 306 (also shown in FIG. 2). Support for the amendments to FIG. 3A can be found in FIG. 2 as originally filed and in the specification from page 3, line 26, through page 4, line 8. Thus, no new matter is introduced. Replacement Sheets (as required by 37 C.F.R. 1.121(d)) are attached to this Amendment.

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Remarks

Applicant and his representatives wish to thank Examiner Ha for the thorough examination of the present application, the detailed explanations in the Office Action dated June 26, 2006, and the very helpful and courteous discussion held with the undersigned on October 3, 2006. The claims and Figure 1 have been amended as discussed. However, FIG. 3A, which shows the bump bonding interface of the invention in greater detail than FIG. 2, has been amended to show the bond pad and Cu pattern, as required in the Office Action. The following remarks shall further summarize and expand upon topics discussed.

Claims 2 and 11 have been canceled. New Claims 19-22 have been added. Thus, Claims 1, 3-10 and 12-22 are active in the present application.

The present invention relates to a method for packaging a semiconductor device, including the steps of (a) forming an Au bump on a bond pad of a wafer, (b) dicing the wafer into a chip, and (c) attaching the Au bump to a copper pattern embedded in a substrate through a plurality of metal layers comprising an Ag layer and a Cu layer to form a flip-chip bond using a thermo-pressure process (see Claims 1 and 10 above).

The cited reference (Coyle et al. [U.S. Pat. Appl. Publ. No. 2002/0084521 A1]) neither discloses nor suggests attaching an Au bump on the bond pad of a wafer to a copper pattern embedded in a substrate through a plurality of metal layers comprising an Ag layer and a Cu layer (see amended Claims 1 and 10 above). Thus, the present claims are patentable over the cited reference.

The Rejection of Claims 1-6 and 10-15 under 35 U.S.C. § 102(b)

The rejection of Claims 1-6 and 10-15 under 35 U.S.C. § 102(b) as being anticipated by Coyle et al. is respectfully traversed.

Coyle et al. disclose structure and method of a Ball-Grid Array or Land-Grid Array plastic integrated circuit (IC) device are described, which have gold bumps on the chip contact

pads, spaced apart by less than 100 μm center to center, flip-chip attached to a thin-film plastic substrate (Abstract, ll. 1-5). Coyle et al. further disclose a chip 104 having an active surface 104a and a passive surface 104b. Active components, forming the IC, are fabricated in active surface 104a, including a plurality of contact pads 105 (Coyle et al., FIG. 1 and p. 3, paragraph [0034]). Electrical coupling members 106 attached to these contact pads are preferably metal bumps selected from a group consisting of gold, copper, copper alloy, or layered copper/nickel/palladium (Coyle et al., FIG. 1 and p. 3, paragraph [0036]).

The coupling members 106 are attached to conductive lines 103 (formed from foil 103) by a thermo-compression bonding technique based on metal interdiffusion (Coyle et al., FIG. 1 and pp. 2-3, paragraphs [0031] and [0038]). The metal foil 103 adheres to an interposer 101 having a first surface 101a (with an adhesive layer 102 thereon) and a second surface 101b (Coyle et al., FIG. 1 and p. 2, paragraph [0031]). Preferred foil materials include copper, copper alloys, gold, silver, palladium, platinum, and stacked layers of nickel/gold and nickel/palladium (Coyle et al., p. 3, paragraph [0033]). As indicated in FIG. 1, the electrically insulating thin-film interposer 101 has a plurality of electrically conductive paths 107 extending through the interposer 101, from its first surface 101a to its second surface 101b. These paths are created by opening vias through interposer 101 (using an etching, laser, or punching technique) and filling these vias either with solderable metal or solder (Coyle et al., FIG. 1 and p. 3, paragraph [0039]). Although Coyle et al. are silent with regard to examples of solderable metal or solder, Coyle et al. teach that solder balls may be selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds (p. 3, paragraph [0039]). Coyle et al. therefore do not appear to disclose attaching an Au bump to a conductive line in a substrate through an Ag layer and a Cu layer.

As a result, Coyle et al. do not disclose attaching the Au bump to a copper pattern embedded in a substrate through an Ag layer and a Cu layer to form a flip-chip bond, as recited in Claims 1 and 10. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

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The Rejection of Claims 7-9 and 16-18 under 35 U.S.C. § 103(a)

The rejection of Claims 7-9 and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Coyle et al. is respectfully traversed.

As discussed above, Coyle et al. is deficient with regard to attaching an Au bump to a copper pattern embedded in a substrate through an Ag layer and a Cu layer, as recited in the present Claims 1 and 10. However, the exemplary stacked layers for metal foil 103 of Coyle et al. do not include silver or copper, and the exemplary solder ball materials of Coyle et al. do not include multi-layer materials. Consequently, Coyle et al. do not suggest to one of ordinary skill in the art attaching an Au bump to a copper pattern embedded in a substrate through an Ag layer and a Cu layer.

Therefore, Coyle et al. do not disclose or suggest all of the limitations of the present Claims 1 and 10, and Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) of Claim 7-9 and 16-18 (which depend directly or indirectly from either Claim 1 or Claim 10).

The Objections to the Drawings

The objections to the drawings have been overcome by appropriate amendment.

Conclusions

In view of the above remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

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If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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